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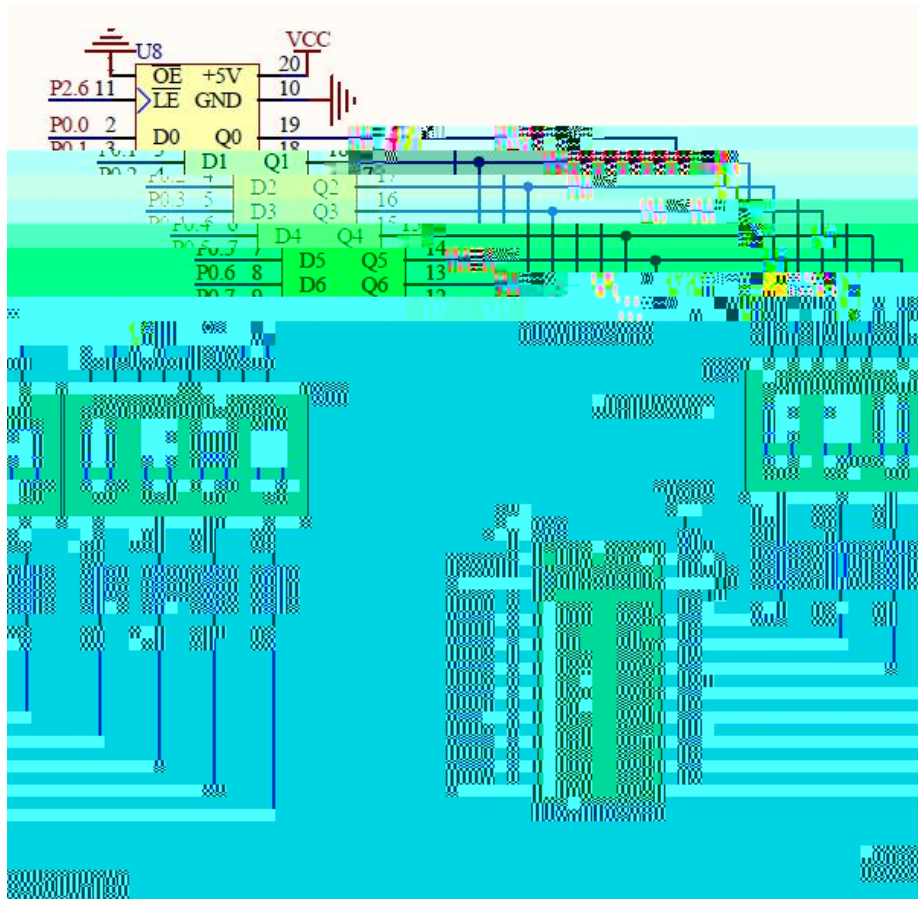








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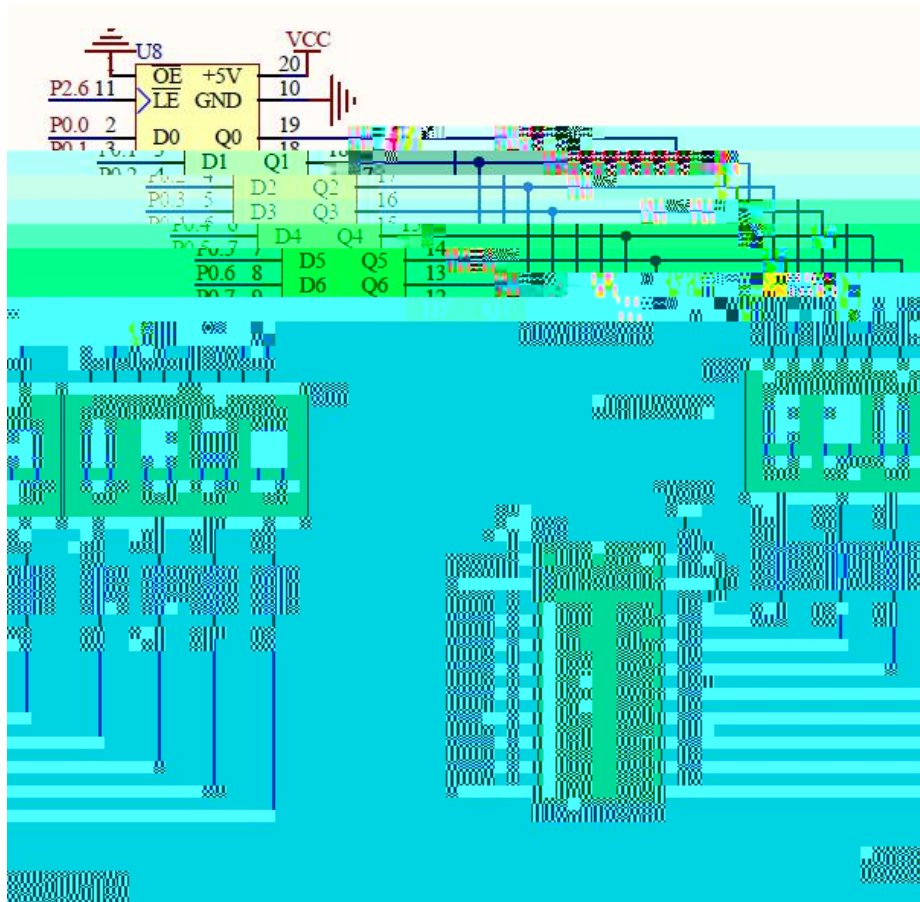
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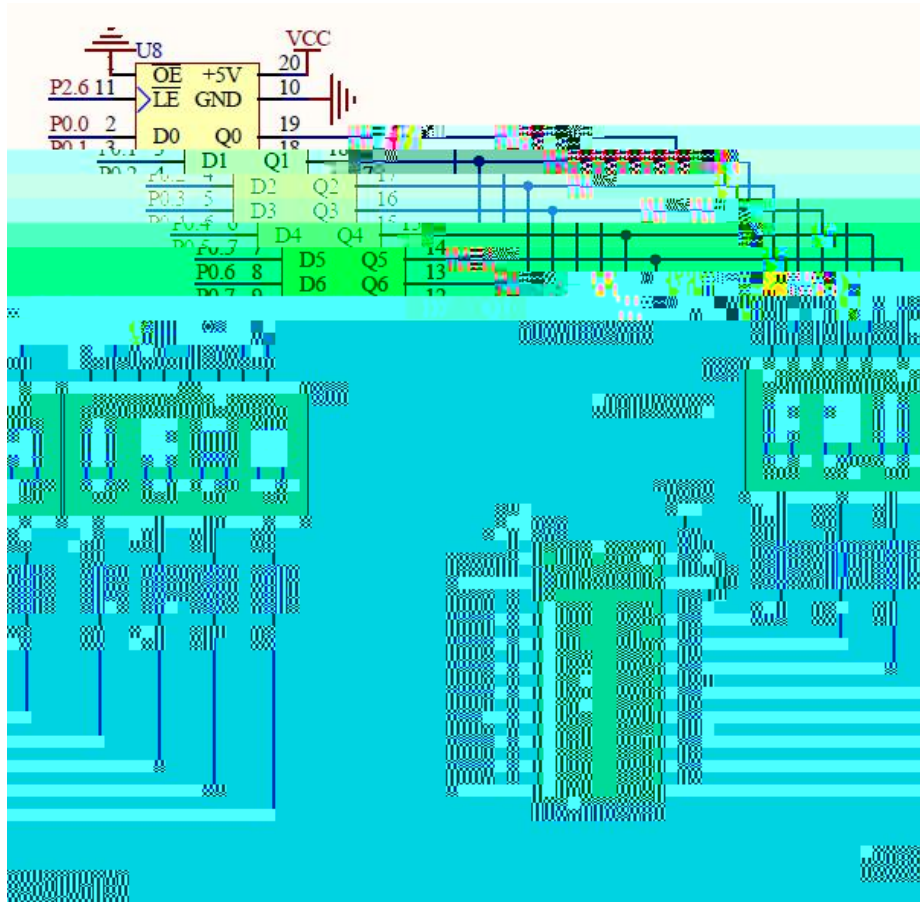
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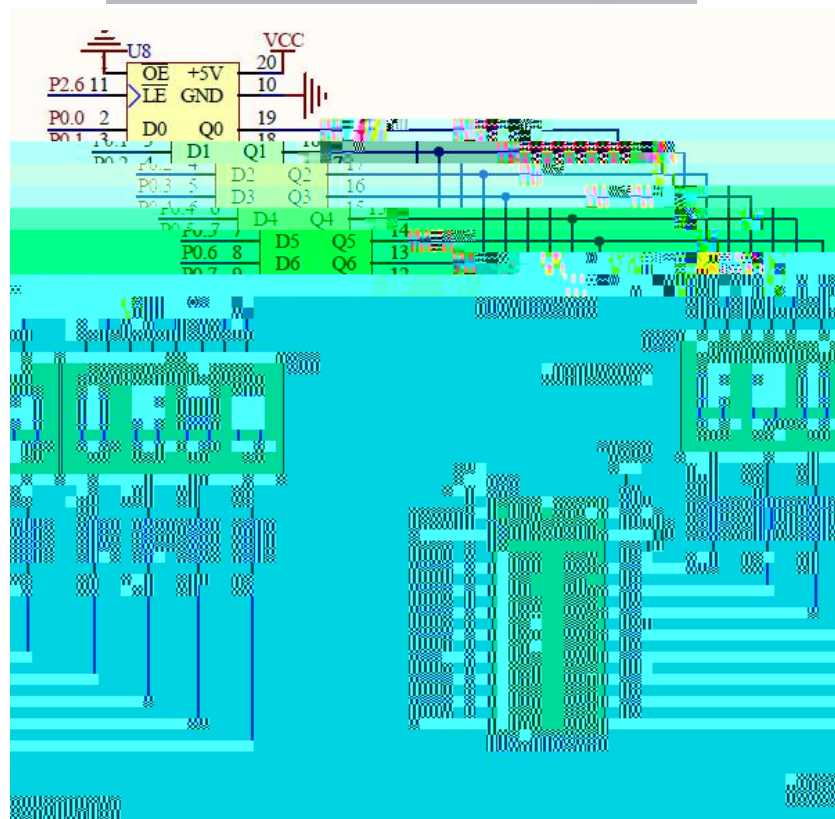
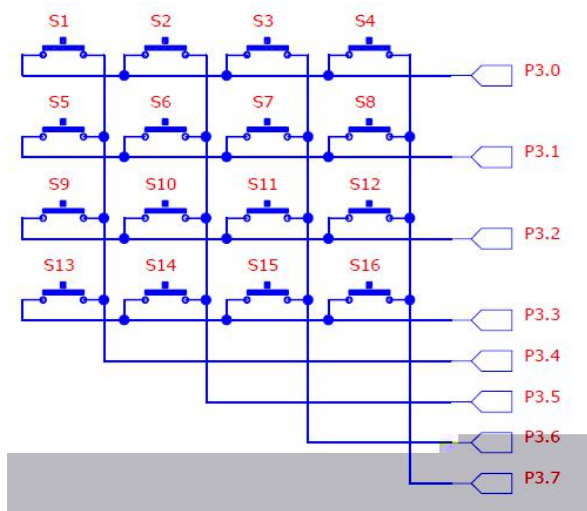
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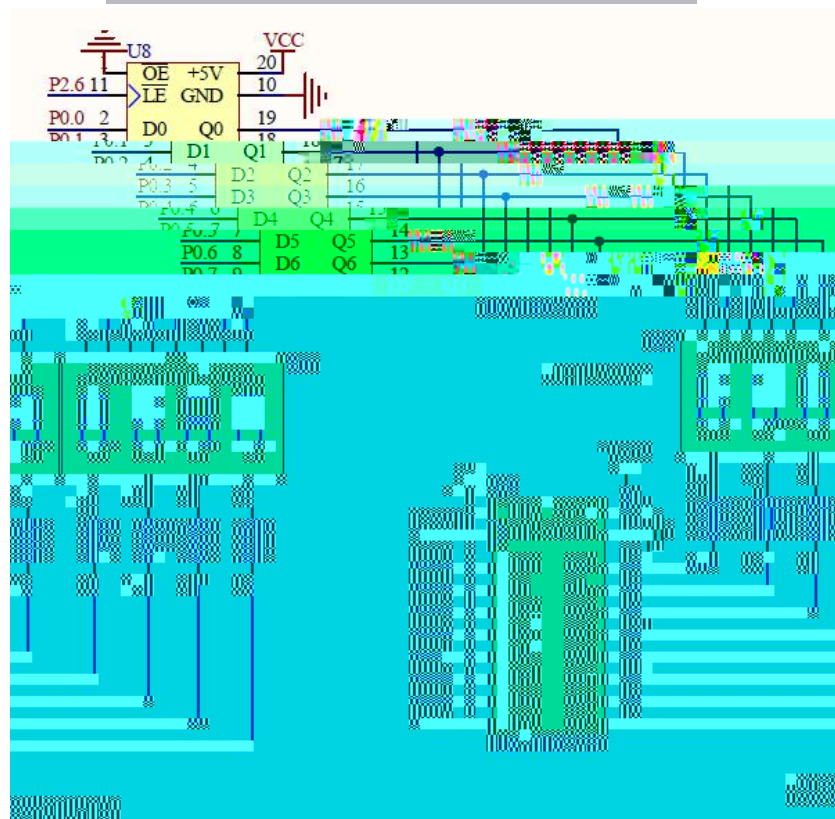
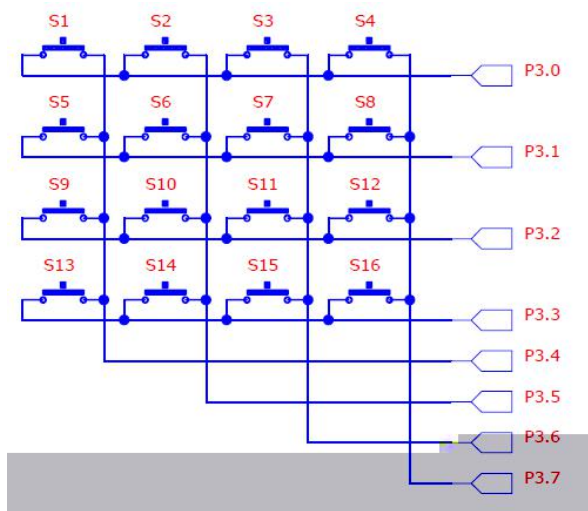
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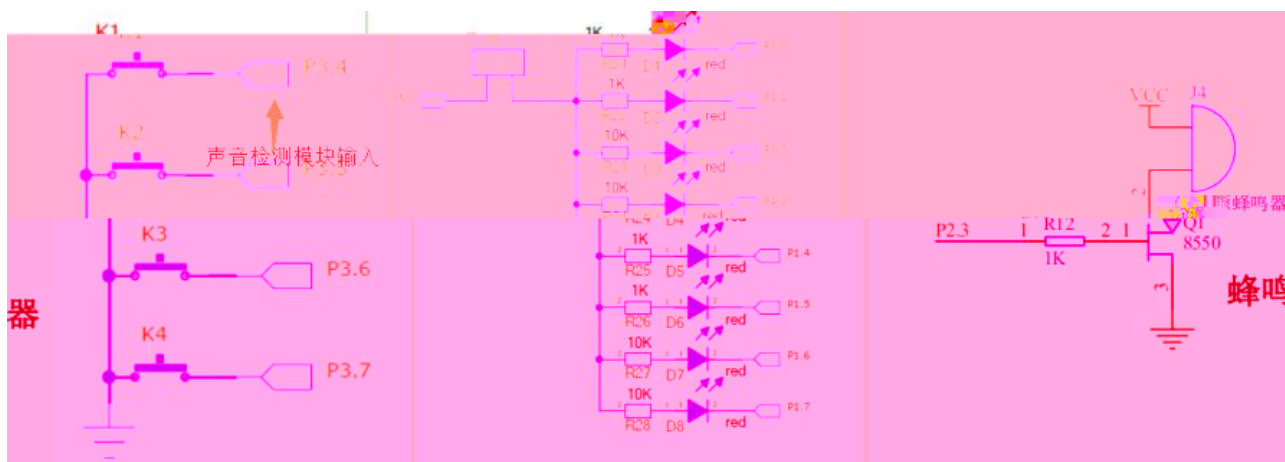
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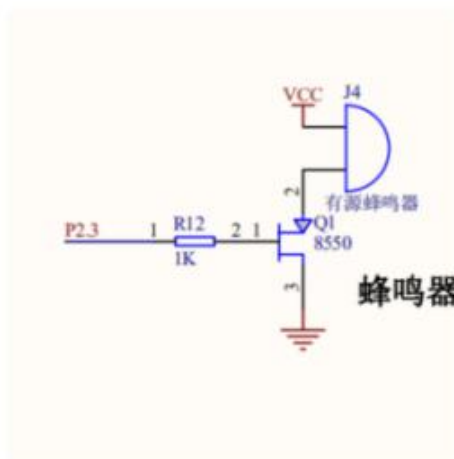
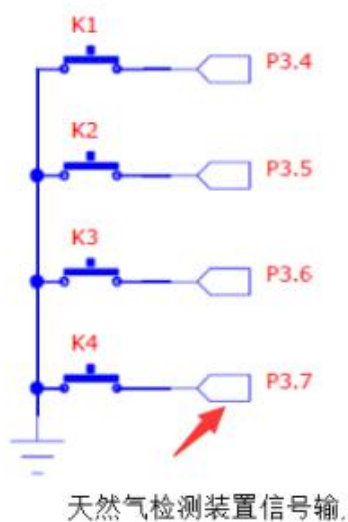
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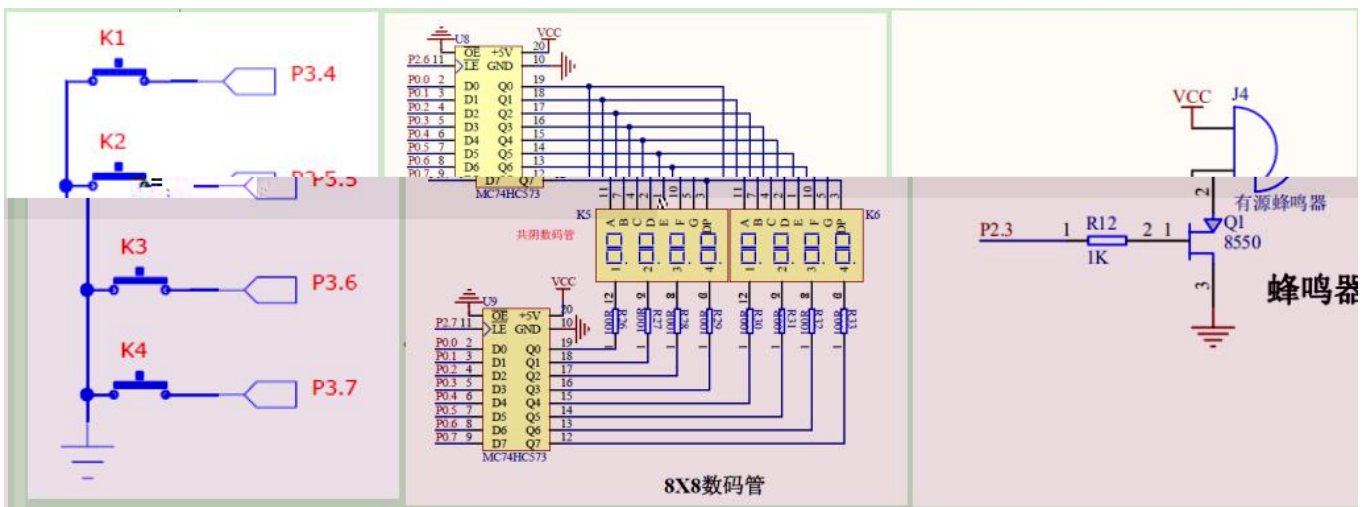
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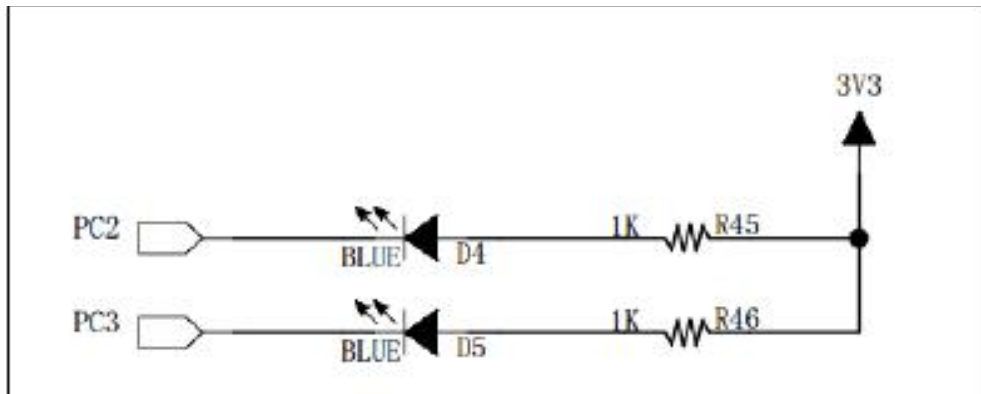
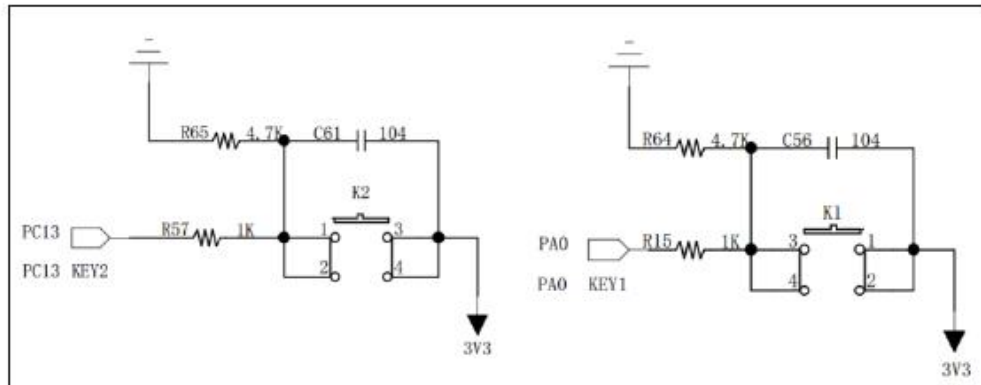
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4	PC15/OSC32	PB8/TIM4_CH3/SDIO_D4	61
5	PD0/OSCIN	...	60
6	PD1/OSCAUT	BOOT0	59
7	NRST	PB7/I2C1_SDA/TIM4_CH2	58
8	PC0/ADC10	PB6/I2C1_SCL/TIM4_CH1	57
9	PC1/ADC11	PB5/I2C1_SMBA/SPI3_MOSI/I2S3_SD	56
10	PC2/ADC12	PB4/JNTRST/SPI3_MISO	55
11	PC3/ADC13	PB3/JTDO/SPI3_SCK/I2S3_CK	54
12	VSSA	PD2/U5_RX/TIM3_ETR/SDIO_CMD	53
13	VDDA	PC12/U5_TX/SDIO_CK	52
14	PA0/WKUP/ADC0/TIM2_CH1_ETR/TIM5_CH1/TIM8_ETR	PC11/U4_RX/SDIO_D3	51
15	PA1/ADC1/TIM2_CH2/TIM5_CH2	PC10/U4_TX/SDIO_D2	50
16	PA2/U2_TX/ADC2/TIM2_CH3/TIM5_CH3	PA15/JTDI/SPI3_NSS/I2S3_WS	49
17	PA3/U2_RX/ADC3/TIM2_CH4/TIM5_CH4	PA14/JTCK/SWCLK	48
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19	VSS	VSS	5
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21	PA5/ADC0/TIM2_CH2/TIM5_CH2	PA12/TIM2_CH2	7
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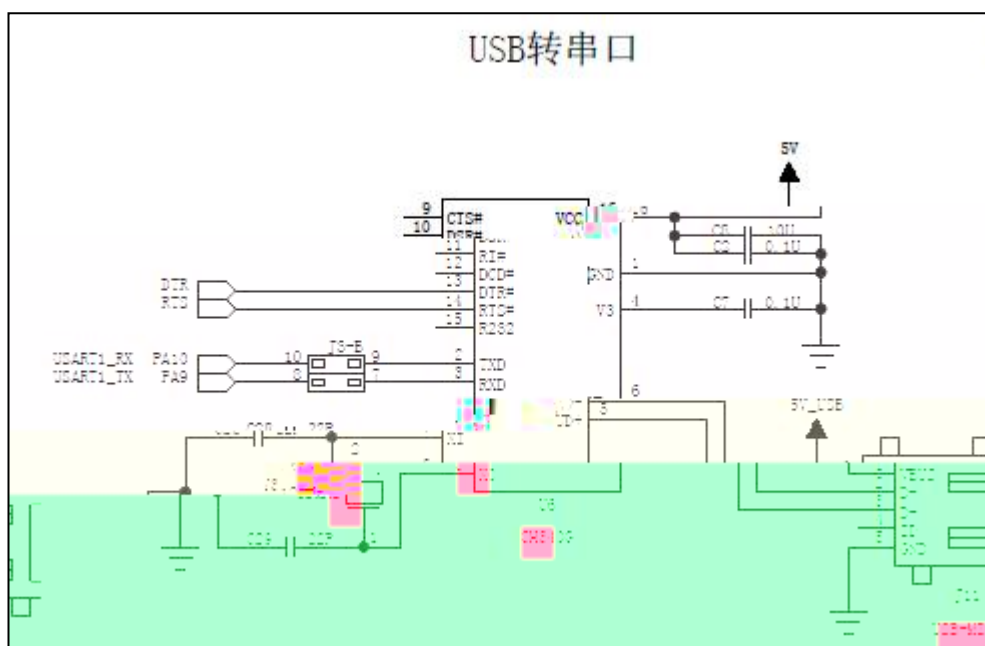
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1	VBAT	VDD	64
2	PC13/ANT1	VSS	63
3	PC14/OSC32	PB9/TIM4_CH4/SDIO_D5	62
4	PC15/OSC32	PB8/TIM4_CH3/SDIO_D4	61
5	PD0/OSCIN	W	60
6	PD1/OSCCOUT	BOOT0	59
7	NRST	PB7/I2C1_SDA/TIM4_CH2	58
8	PC0/ADC10	PB6/I2C1_SCL/TIM4_CH1	57
9	PC1/ADC11	PB5/I2C1_SMBA/SPI3_MOSI/I2S3_SD	56
10	PC2/ADC12	PB4/JNTRST/SPI3_MISO	55
11	PC3/ADC13	PB3/JTDC/SPI3_SCK/I2S3_CK	54
12	VSSA	PD2/U5_RX/TIM3_ETR/SDIO_CMD	53
13	VDDA	PC12/U5_TX/SDIO_CK	52
14	PA0/WKUP/ADC0/TIM2_CH1_ETR/TIM5_CH1/TIM8_ETR	PC11/U4_RX/SDIO_D3	51
15	PA1/ADC1/TIM2_CH2/TIM5_CH2	PC10/U4_TX/SDIO_D2	50
16	PA2/U2_TX/ADC2/TIM2_CH3/TIM5_CH3	PA15/JTD/SPI3_NSS/I2S3_WS	49
17	PA3/U2_RX/ADC3/TIM2_CH4/TIM5_CH4	PA14/JTCK/SWCLK	48
		VDD	4
18	PC4	VDD	3
19	PC5	PA13/TIM8_ETR	2
20	PC6	PA12/CKI/TIM8_ETR	1
21	PC7	PA11/CKE/SDIO_CMD	0
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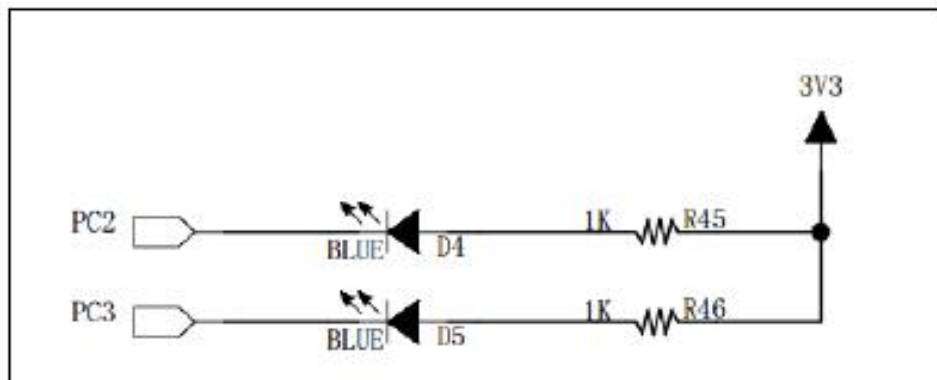
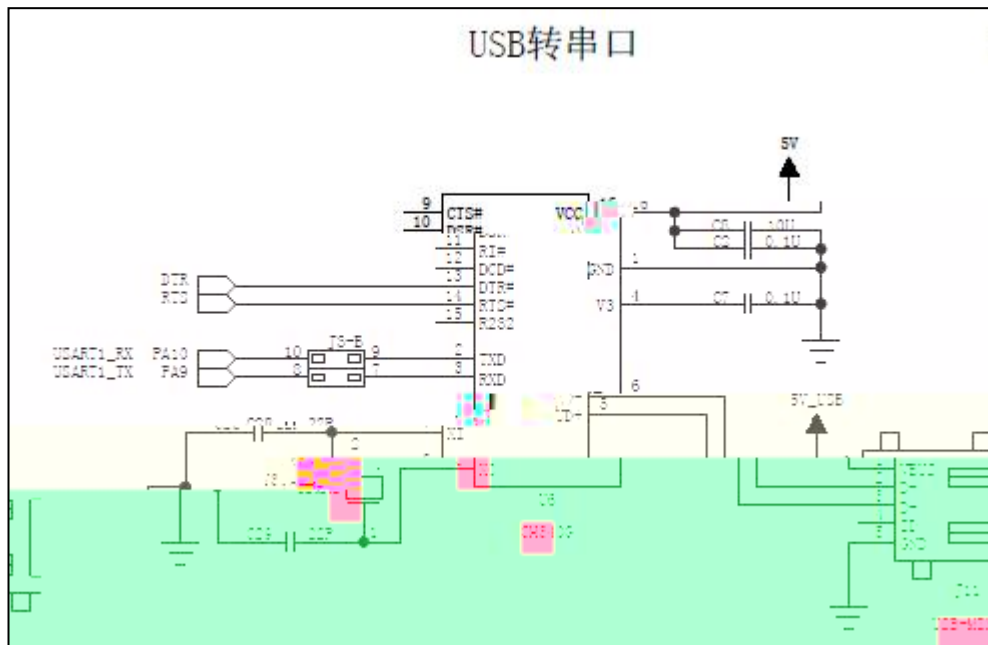


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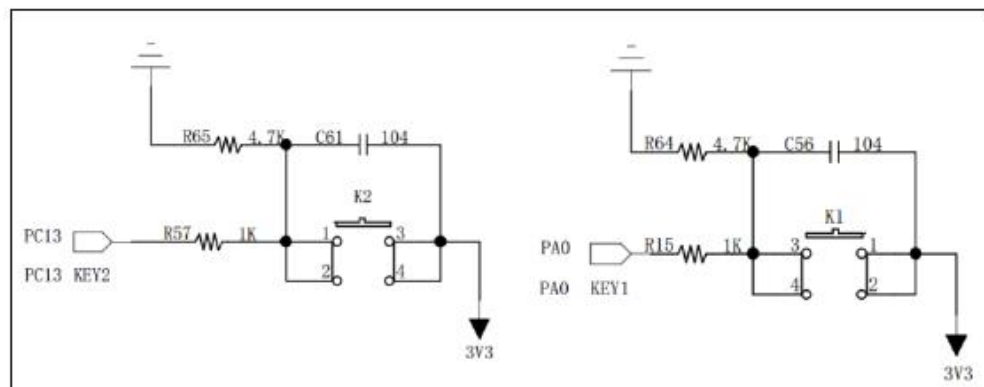
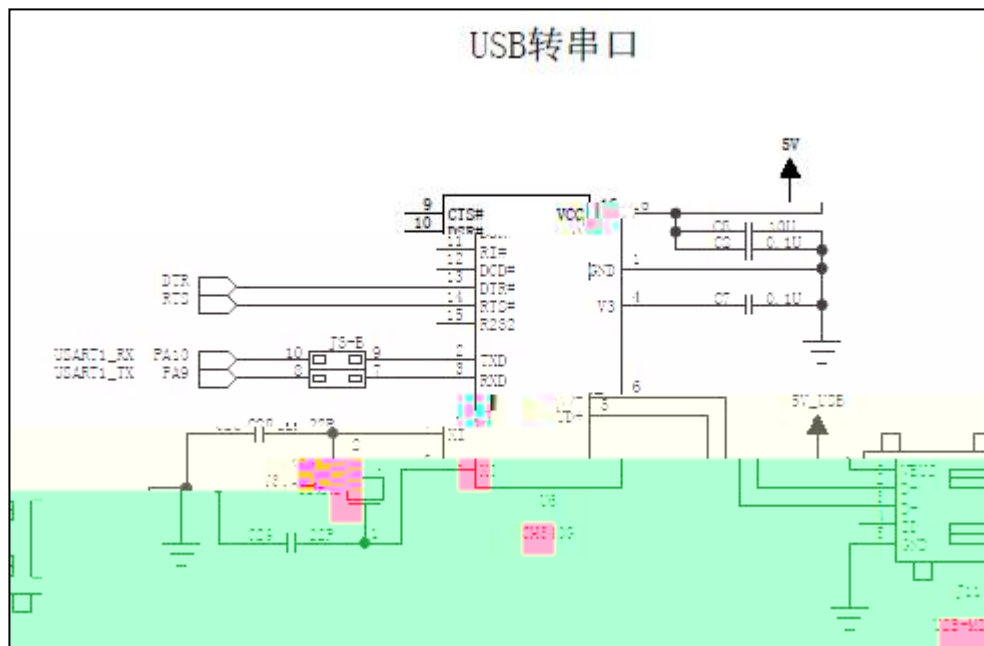


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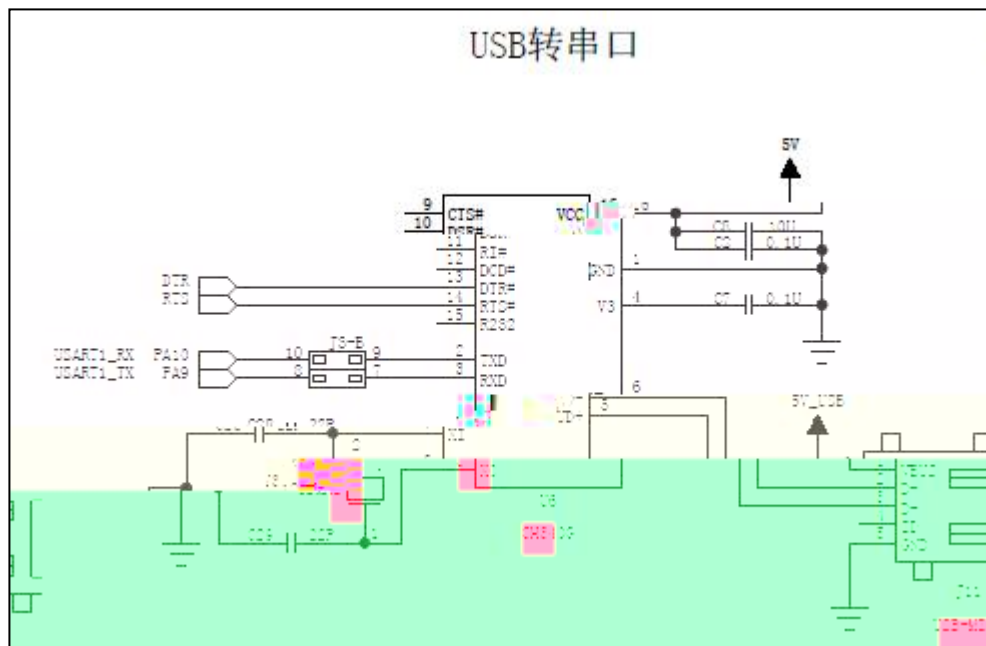


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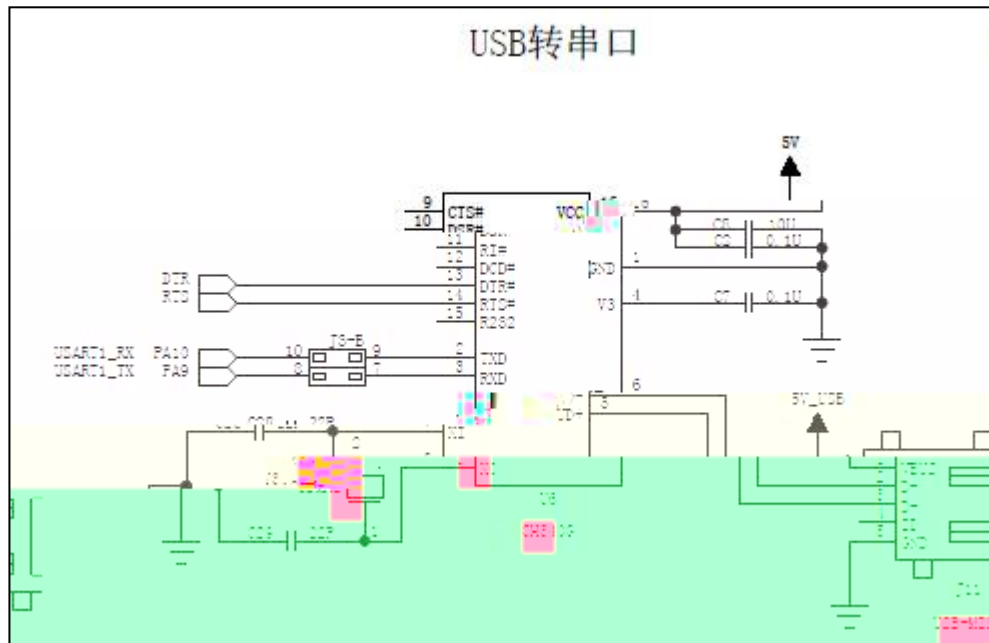
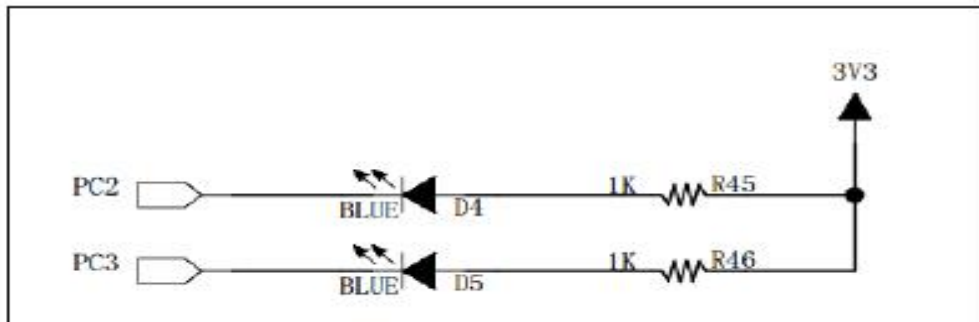


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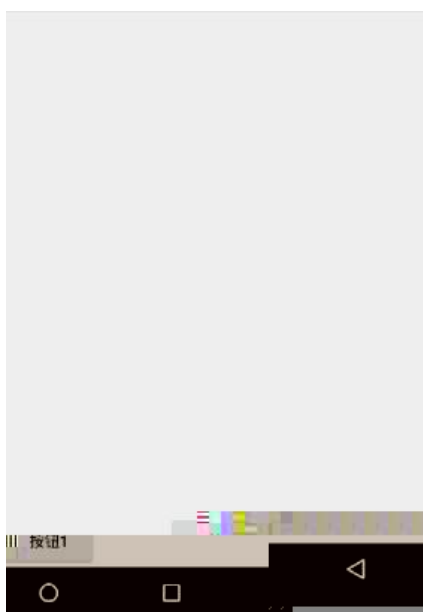
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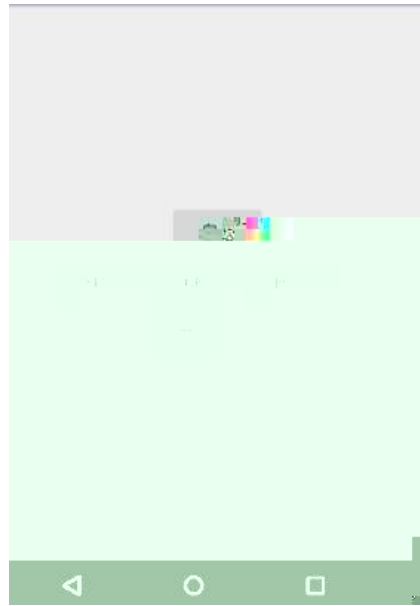


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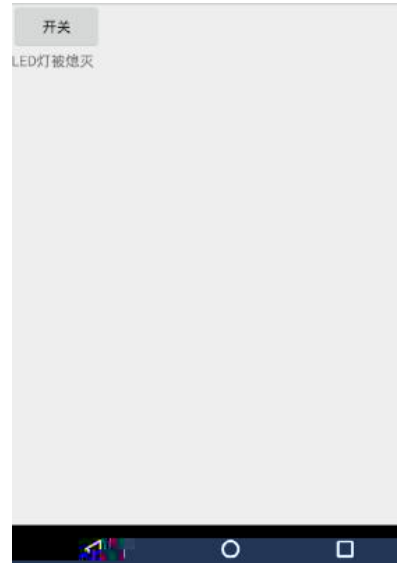
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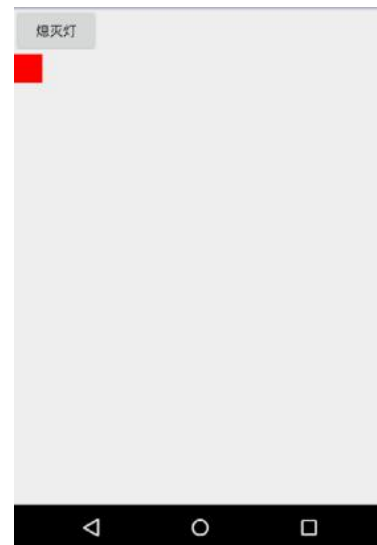
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